REMARKS

This amendment is submitted in response to the Examiner's Action dated January 23, 2006. Applicants have amended the claims to clarify key features of the invention and overcome the claim objections and rejections. No new matter has been added, and the amendments place the claims in better condition for allowance. Applicants respectfully request entry of the amendments to the claims. The discussion/arguments provided below reference the claims in their amended form.

CLAIMS OBJECTIONS

In the present Office Action, Claims 1-20 are objected to because of informalities. Accordingly, Applicants have amended Claims 1-20 to remove the stated informalities and overcome the claim objections. Notably, Applicants are unclear what Examiner is referring to at paragraph 7 of the Office Action, but believe the present amendments should overcome all objections. Applicants thus respectfully request removal of the objections to the claims.

CLAIMS REJECTIONS UNDER 35 U.S.C. § 112

In the present Office Action, Claims 1-20 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Applicants have amended the claims to remove all stated indefiniteness. The claims now recite definite features and thus the amendments overcome the §112 rejection. Applicants respectfully request reconsideration and removal of the §112 rejection in light of the amendment.

CLAIMS REJECTIONS UNDER 35 U.S.C. § 102

In the present Office Action, Claims 1, 2, 3 and 8-10 are rejected under 35 U.S.C. § 102(a) as being anticipated by *"Multiplexers and Demultiplexers"* (hereinafter *"Multiplexers"*). Claims 12, 15 and 18 are rejected under 35 U.S.C. §102(a) as being anticipated by *Maejima* (U.S. Patent No. 6,639,848). Neither reference teach the specific features recited by Applicants' claims, and thus, neither reference anticipates Applicants' claimed invention.

With respect to *Multiplexers*, Examiner incorrectly attributes to that reference several features recited within Applicants' claims which are neither taught nor suggested by *Multiplexers*. Among these features are the following:

(1) a first latch having a single data input port and a single clock input port and an output port;

(2) a second latch also having a single data input port and a single clock input port and an output port;

(3) means for ... **selection of a scan chain input at said first latch and said second latch;**

(4) means ... selection of a shift chain input at said first latch and said second latch; and

(5) wherein a selection of the scan chain input ... occurs exclusive of selection of the shift chain input..., and wherein said single data input latches provide functionality of latches that support multiple inputs.

Multiplexer simply provides an N-to-1 MUX configuration with two select inputs (c1 and c0) utilized to trigger a connection of three MUXes, each having two data inputs. The MUXes provided by *Multiplexer* operate as standard MUXes with two data inputs and a select input. Applicants' invention clearly provides fuses, latches, and other circuit components that are coupled together and eventually feed two inputs to a MUX. It is therefore clear that *Multiplexer* fails to teach the above listed and other features of Applicants' more complex circuit device.

Maejima likewise fails to teach (or suggest) key features recited by the other independent claims. In fact *Maejima* does not even teach (or even contemplates or suggests) a method or means for "selectively accepting the scan chain input into said latch to commence a scan chain operation within said device only when a first clock input is on; and means for alternatively accepting the shift chain input into said latch to commence a shift chain operation within said device only when a second, different clock input is on, wherein only one clock signal is on at a time and both said scan chain operation and said shift chain operation are supported by said single input, scan only latch."

Maejima is primarily concerned with providing a redundancy circuit on a nonvolatile memory device (Abstract). The cited section of *Maejima*, namely col. 2, ll 54-64 describes "a test flow for the conventional redundancy circuit replacement" (ll 53-54) and provides for completing a DS test to check for defects in the chip and shifting to a eFuse blowing step for redundancy circuit replacement if the defect chip is retrievable (paraphrasing ll 54-64). Clearly,

this description is not synonymous with or suggestive of the features recited by Applicants' claims.

The standard for a § 102 rejection requires that the references teach each element recited in the claims set forth within the invention. As clearly outlined above, both references fail to meet this standard and therefore neither reference anticipates Applicants' invention.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103

In the present Office Action, Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Multiplexers* as applied to Claim 3 above, and further in view of *Esposito* (U.S. Patent No. 4,066,882). Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Multiplexers*. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Multiplexers* as applied to Claim 3 above, and further in view of *Esposito* (U.S. Patent No. 4,066,882). Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Multiplexers* as applied to Claim 9 above, and further in view of *Maejima*. Claims 13, 14, 16, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Maejima*.

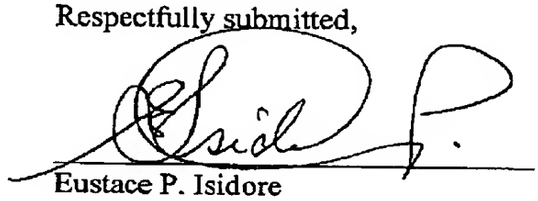
Each of these claims depend from one of the independent claims, which Applicants have shown to be allowable over the references being utilized as primary references to support the present §103 rejection. Since the present claims depend from allowable claims, these claims are also allowable over the references and combinations thereof.

CONCLUSION

Applicants have diligently responded to the Office Action by amending the claims to overcome claim objections, and §112 rejections, and to clarify features within specific claims. Applicants have also provided discussion/arguments which show why Applicants' claims are not anticipated by or obvious in light of the references provided. Since the amendments and arguments overcome the §§ 112, 102 and 103 rejections, Applicants, respectfully request issuance of a Notice of Allowance for all claims now pending.

Applicants further respectfully request the Examiner contact the undersigned attorney of record at 512.343.6116 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,



Eustace P. Isidore
Reg. No. 56,104
Dillon & Yudell LLP
8911 North Capital of Texas Highway
Suite 2110
Austin, Texas 78759
512.343.6116

ATTORNEY FOR APPLICANT(S)